

# CRYSTALLISATION OF PURIFIED METALLURGICAL SILICON

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## ABSTRACT

The crystallization of purified metallurgical Silicon often leads to multi crystalline ingots which present regions of strong compensation and an inversion of the polarity type. These effects result from the presence of different dopant atoms, donors and acceptors, in this type of Silicon and their different segregation behavior during the crystallization process. The most commonly found dopant atoms in Silicon, Boron and Phosphorous, have relatively high segregation coefficients with an important difference in their absolute value. As a result, suitable resistivities in the 0.5 to 1.0  $\Omega\text{cm}$  range are obtained in an important part of the ingot, but at a relatively high compensation ratio. This paper discusses these compensation effects, as observed on upgraded metallurgical Silicon from the PHOTOSIL project [1] and using a new crystallization process and furnace developed by CYBERSTAR and APOLLONSOLAR [2].

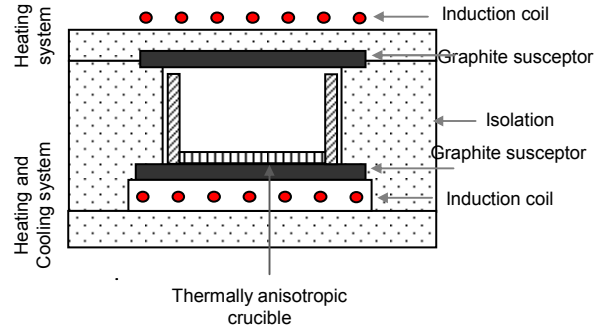
## INTRODUCTION

In times of a strong and sustainable economic growth to the Silicon based PV industry, the increasing demand for Silicon feedstock of suitable quality has led to a drastic price increase and shortage of the classical Silicon feedstock. Numerous initiatives are under way to increase the production of a pure Silicon feedstock using chemical purification techniques, which are known from the production of electronic grade Silicon. At the same time, other initiatives have started to explore the purification of metallurgical grade Silicon to arrive at a quality level that is compatible with the requirements of the PV industry at a much lower cost scenario. The French PHOTOSIL project is one of the latter initiatives. In order to be able to use purified metallurgical grade Silicon for PV applications on an industrial scale, an increased understanding of the behavior of this material during the major processing steps, such as multi-crystalline ingot crystallization and solar cell processing is required.

## CRYSTALLISATION EQUIPMENT

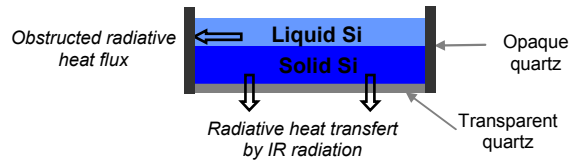
The crystallization furnace features a very uniform heating and cooling system, consisting of two independently controlled inductive heating elements, one situated above, the other below the crystallization crucible, with the water cooled inductive coil of the bottom system

serving at the same time as heat exchanger, see also Figure 1.



**Figure 1:** Schematic view of thermal elements in the CYBERSTAR crystallization furnace.

In addition, the crucible used for this crystallization process, shows a thermally anisotropic characteristic in that its bottom plate is made of transparent quartz and its side walls of opaque quartz as shown in Figure 2.



**Figure 2:** Thermally anisotropic quartz crucible used for the crystallization of multi crystalline ingots.



**Figure 3:** Photo of an anisotropic quartz crucible with transparent bottom and opaque side walls.

This anisotropic quartz crucible, as shown in Figure 3, allows for a preferred heat extraction through its transparent bottom via infrared radiation, whereas the opaque crucible walls block radiative heat transfer and thus support lateral insulation. As has been shown in [2] the maximum emittance of Silicon coincides with the transmittance window of the transparent quartz. The combination of both, thermal furnace components and the crucible allow thus for high temperature gradients ( $>20\text{K/cm}$ ) at the solid/liquid interface to be established and to obtain a perfectly planar and stable solidification front during crystallization. As can be seen on the photo of a vertical cut of an ingot presented in Figure 4, the obtained grain structures are vertical. Both conditions are essential for an efficient segregation of impurities during crystal growth, which is especially important for the crystallization of lower quality Silicon such as upgraded metallurgical Silicon.

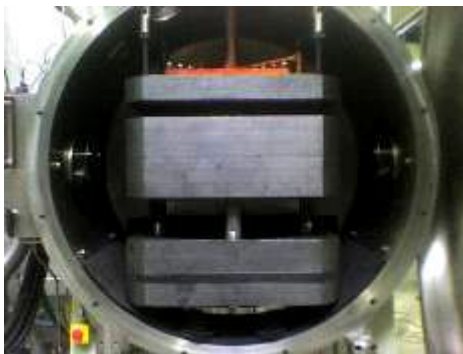


**Figure 4 :** Vertical grain structures on a vertical cut from a multi-crystalline Silicon ingot

## EXPERIMENTAL RESULTS

### a) Crystallisation

Crystallisation experiments were carried out in a laboratory scale and an industrial scale CYBERSTAR crystallisation furnace, using the above described thermal configuration. The industrial scale furnace is installed in the PHOTOSIL pilot line and shown in Figure 5.



**Figure 5:** Industrial scale CYBERSTAR crystallisation furnace used in the PHOTOSIL pilot line. The thermal insulation surrounding the crucible is visible in the middle.

The upper and lower susceptors, also surrounded by insulating elements have been lifted and lowered, respectively, to be able to remove the crucible and surrounding insulation.

Comparative crystallisation experiments have been carried out, using two different types of Silicon: (i) Electronic grade (EG) Silicon which was doped with 1ppma of Boron in order to obtain p-type Silicon with a resistivity of  $0.5\Omega\text{cm}$ ; (ii) Purified metallurgical grade (SoG) Silicon from the PHOTOSIL project with remaining impurity concentrations as shown in Table 1. This material is of intermediate quality but interesting for experiments destined for gaining further understanding in the compensation behaviour.

**Table1:** Impurity concentrations in purified metallurgical grade Silicon used for the crystallisation experiments, as obtained by ICP. This Silicon is an intermediate material and not representative. The concentrations of Al and Cu are below the detection limit.

Element	B	P	Al	Fe	Cu
C [ppmw]	2.9	5.5	<5	26	<2

The two resulting 6 kg test ingots have been cut into wafers and electrically characterised in terms of resistivity, Hall mobility and carrier lifetime, the latter one was determined by QSSPC with methanol/iodine passivated surfaces and the light bias function was used in order to correct for trapping effects. The characterisation results are summarised in Table 2.

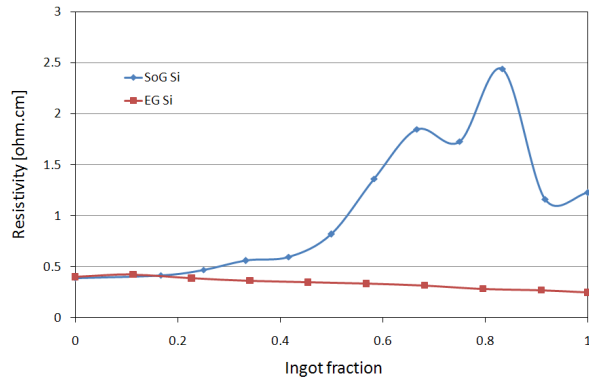
**Table 2:** Carrier lifetimes, Hall mobilities and resistivities of the ingots grown from EG Silicon and purified MG (SoG) Silicon.

	Hall Mobility ( $\text{cm}^2/\text{V.s.}$ )		Minority carrier Lifetime ( $\mu\text{s}$ )		Resistivity ( $\Omega\text{cm}$ )	
	SoG	EG	SoG	EG	SoG	EG
<b>Bottom</b>	160	180	2	2	0.3	0.5
<b>Middle</b>	160	280	4.5	7.5	0.8	0.5
<b>Top</b>	50	180	-	3	1.5	0.4

As can be seen, the resistivity of the SoG ingot increases from the bottom to the top, whereas it is uniform around  $0.5\Omega\text{cm}$  in case of the EG ingot, see also Figure 6, showing the resistivity as a function of the ingot height.

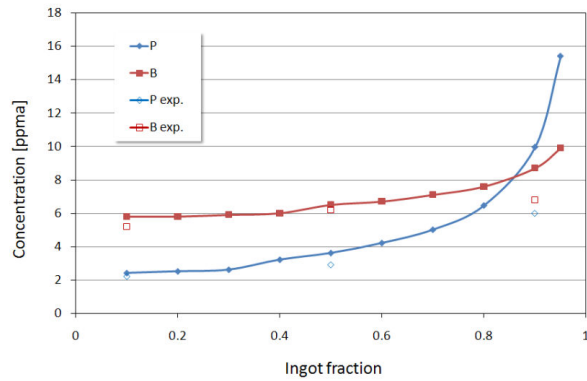
The phenomenon of increasing resistivity with increasing ingot height is usually observed in compensated Silicon. This is due to the Phosphorous which is still present in the purified metallurgical grade Silicon and has segregated during crystal growth towards the top region of the ingot, resulting in a region of high

resistivity starting from 75% of the maximum ingot height.



**Figure 6:** Resistivity as a function of ingot height for the two ingots grown from electronic grade (EG) Silicon and purified metallurgical (SoG) Silicon.

Figure 7 compares concentrations of Phosphorous and Boron obtained by chemical analysis on wafer level with calculated segregation curves, using the Scheil equation and the respective impurity concentrations analysed in the purified metallurgical Silicon.



**Figure 7:** Calculated and measured distribution of P and B showing the difference in segregation behaviour and the appearance of the n-type zone.

The n-type region at the top of the ingot is characterised by a very low carrier lifetime. In general, carrier lifetimes and Hall mobilities are lower in the ingot from purified metallurgical grade Silicon, as shown in Table 1, which is also due to compensation effects and probably a higher defect density. These defects might have been induced by remaining impurities acting as nucleation centres. The presence of defects is supported by the observation of trapping effects while measuring the carrier lifetimes of this ingot by QSSPC.

Comparing Figures 6 and 7 it becomes evident that the change of polarity type according to the electrical

characterization in Figure 6 and following the segregation of Phosphorous and Boron in Figure 7 does not take place at the same ingot position. This might indicate that other dopant atoms are also involved in the ingot from purified metallurgical grade Silicon.

It has been found that the obtained doping concentration  $N_A-N_D$  does not correspond to the measured resistivity, which indicates a potential detrimental effect of compensation effects on the mobilities, probably due to scattering effects at ionized dopants.

Table 2 summarises measured Hall mobilities and measured net dopant concentrations  $N_A-N_D$  for a fixed resistivity of  $0.45\Omega\text{cm}$  that has been found on wafers from both, the electronic grade (EG) Silicon ingot, and from the compensated purified metallurgical Silicon ingot. These measured values are compared to the theoretical values, from PC1D. In the case of the compensated Silicon, a much lower mobility and higher doping density gives rise to the same resistivity as in the case of electronic grade Silicon. The difference in mobility between the theoretical values and the electronic grade Silicon is due to scattering effects at grain boundaries and other crystalline defects in the electronic grade ingot. The dopant density of the electronic grade Silicon is very close to the theoretical value.

**Table 2:** Comparison of measured Hall mobilities, net dopant concentrations  $N_A-N_D$  and theoretical values with a fixed resistivity of  $0.45\Omega\text{cm}$ .

	Theoretical (PC1D)	EG-Silicon	Compensated Silicon
$\rho$ [ $\Omega\text{cm}$ ]	0.45	0.45	0.45
$\mu$ [ $\text{cm}^2/\text{Vs}$ ]	378	285	124
$N_A-N_D$ [ $\text{cm}^{-3}$ ]	$3.67 \times 10^{16}$	$5.0 \times 10^{16}$	$1.06 \times 10^{17}$

In addition, the strongly compensated regions are characterized by a surprisingly high minority carrier diffusion length in the order of  $120\mu\text{m}$ , as obtained by LBIC analysis on solar cells.

### b) Solar Cells

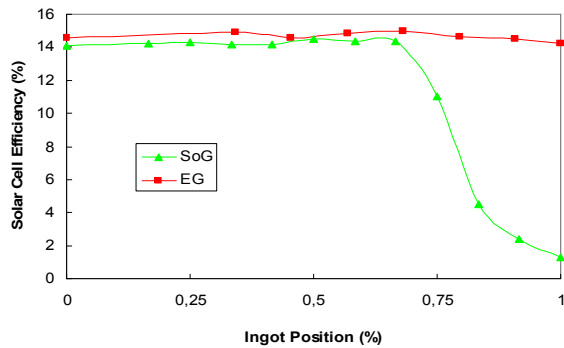
Solar cells have been processed on wafers from both ingots using an industrial type standard process at the CEA-INES Restaure pilot line [3]. Cells from the p-type region of the SoG Silicon ingot have reached an average efficiency of 13.8 % including a best cell with 14.0 %, see also Table 3. The cells from the EG Silicon ingot have

reached average efficiencies of 15%, which are uniformly distributed from the bottom to the top of the ingot, see Figure 8.

**Table 3:** Results of solar cells from the ingot using purified metallurgical Silicon.

	$J_{sc}$ [mA/cm <sup>2</sup> ]	$V_{oc}$ [mV]	FF [%]	$\eta$ [%]
SoG av.	29.5	612	76.4	13.8
SoG best	29.5	611	77.6	14

It has to be noted that the solar cells from the purified metallurgical grade Silicon suffer from light induced degradation (LID). The efficiencies indicated in Table 3 are the ones obtained before LID. A decrease of the efficiency of about 0.6 % absolute was observed after illumination for cells from the bottom part of the SoG ingot.'



**Figure 8:** Solar cells efficiencies as a function ingot height for the ingots from EG Silicon and purified metallurgical grade (SoG) Silicon.

### CONCLUSIONS

A new crystallization furnace and process with a very uniform heating and cooling system allows for the crystallization of multi crystalline Silicon ingots with an effective segregation of remaining impurities as found with purified metallurgical grade Silicon.

This type of Silicon often shows compensation effects related to the difference in segregation behavior of remaining dopant atoms, such as Phosphorous and Boron. Among the beneficial effects related to compensation are the fact that a higher total doping concentration can be accepted to obtain a desired resistivity and that compensated regions often show high minority carrier diffusion lengths. On the other hand, detrimental effects related to compensation, such as lower majority carrier mobility and a polarity type change at a

certain ingot height limiting material yield have to be cited as well.

### ACKNOWLEDGEMENTS

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