NEW METHOD FOR GRAIN SIZE CHARACTERIZATION OF A MULTI-CRYSTALLINE SILICON INGOT

M. Forster[1], E. Fourmond[1]*, J.M. Lebrun[1], R. Einhaus[2], J. Kraiem[2], M. Lemiti[1]
1: INSA de LYON, INL, 7 av. J. Capelle, 69621 VILLEURBANNE CEDEX
2: APOLLON SOLAR, 23 rue Claudius Collonge, 69002, Lyon, France
*Corresponding Author: Tel: +33 4.72.43.82.33, Fax: +33 4.72.43.85.31, E-mail: erwann.fourmond@insa-lyon.fr

ABSTRACT: In order to estimate the quality of the crystallisation process of multi-crystalline Silicon ingots, we have developed a new optical method for the determination of grain sizes on as-cut wafers that were taken from different height positions of the ingot. This fast method is based on image analysis and allows in a simple way to get numerical data which represent the crystallographic quality of silicon wafers. The obtained data were used to calculate a grain size distribution over the analysed wafer area as well as an average grain size by using two different algorithms. It was thus possible to represent the average grain size as a function of ingot height, which indicates ingot regions of lower crystalline quality, for example regions of equiaxed growth of very small grains ("grit"). This technique was used for the characterisation of different multi-crystalline Silicon ingots, using Silicon feedstock of different quality (electronic, upgraded metallurgical or solar grade), and also to monitor the impact of modifications of the crystallisation process parameters on the grain sizes distribution. It was found that this method is able to give a first qualitative impression of the multi-crystalline ingots and wafers which in the end are used to produce solar cells.
Keywords: crystallization, silicon, grain.

1 INTRODUCTION

Multi-crystalline Silicon (mc-Si) is the material with the largest market share in photovoltaic cells and modules production. Mc-Si is usually produced in form of square shaped ingots that are crystallized by directional solidification of molten Silicon feedstock. The obtained ingots are cut into bricks and wafers, which are then used for the processing of solar cells.

The quality of mc-Silicon wafers in terms of electrical performance depends on both, the purity of the Silicon feedstock, i.e. the concentration of remaining impurities, and the crystalline quality of the ingots. The latter is strongly related to the crystallization process itself; however the impurity content in the Silicon can be of a certain influence. This work focuses on crystal defects that result from the crystallisation process itself, which is of relative importance on the degradation of the electrical performance of the material, especially when these defects become highly recombinant due to decoration with impurities.

We have developed a simple optical method to quantify the crystallization quality of mc-Si wafers by an image analysis routine and the treatment of numerical data. Similar methods already exist in the field of metallurgy, but are used to measure micrometric grains and require optical and/or secondary electron microscopy [1], or even use the electron backscattering diffraction (EBSD) technique [2]. Our aim is to measure the grain sizes over the entire surface of a wafer, typically 125×125 mm² in dimension, with a simple and fast method. We present here some typical results obtained with our method on a directional crystallisation process, specially developed by Cyberstar and Apollonsolar.

2 CRYSTALLIZATION PROCESS PRESENTATION

Three different qualities of silicon have been crystallized in this study: Electronic grade (EG), conventional solar grade (SoG) and upgraded metallurgical grade silicon (UMG). The crystallization process has been carried out in a furnace developed by Cyberstar and Apollonsolar, which has already been presented [3,4] and is shown in Figure 1. The process is similar to a directional solidification, Bridgman-type. However the furnace used in this study comports two major improvements, which are briefly presented in the following.

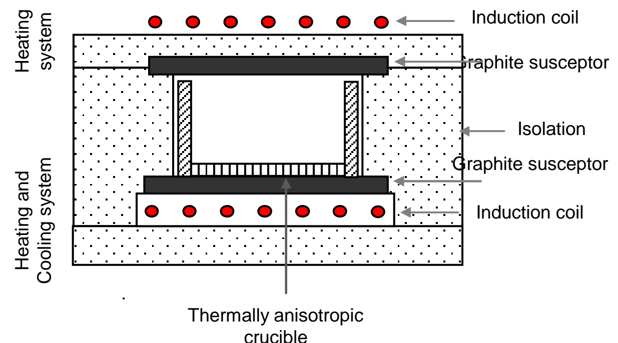

Figure 1: Schematic view of the configuration of the Cyberstar/AS crystallisation furnace.

This furnace features two independently controlled inductive heating elements, and a quartz crucible with a transparent bottom plate. This configuration results in a preferred heat transfer by infrared radiation through the crucible bottom during the crystallization process. The thermal configuration of both, furnace and crucible allows thus high temperature gradients at the solid/liquid interface to be established and controlled during the solidification step. The purpose is to obtain a perfectly planar and stable solidification front during crystallization, from bottom to top. Both conditions are essential for an efficient segregation of impurities during crystal growth, which is especially important for the crystallization of lower quality Silicon such as upgraded metallurgical Silicon. The control of the temperature gradient permits also a better control of the germination process, and hence an improvement in the grain size on the mc-Si

substrate.

3 OPTICAL CHARACTERIZATION OF THE WAFER

After solidification, the ingot is cut into wafers. The characterisation method presented here consists of the digitization of the wafer surface by an optical scanner. The obtained image (Figure 2-a) is then treated with a succession of functions using the ImageJ public domain and open source software [5].

3.1 Method

The ImageJ treatment enables us to get a binary picture (Figure 2-b), with the grain area being black and the grain boundaries being white, which allows to determine the surface of each grain by counting the number of pixels within each grain. Images are shown before and after ImageJ treatment in Figure 2. It is important for the measurement that the surface of the wafer is clean. To guaranty a precise measurement, it is advantageous to work with anisotropically textured wafers, obtained with KOH chemical etching for instance. This ensures a strong optical contrast between the different grains, and thus allows better recognition of grain boundaries. The obtained data are then treated with a spreadsheet to calculate the average grain size and the distribution of different grains sizes over the wafer surface.

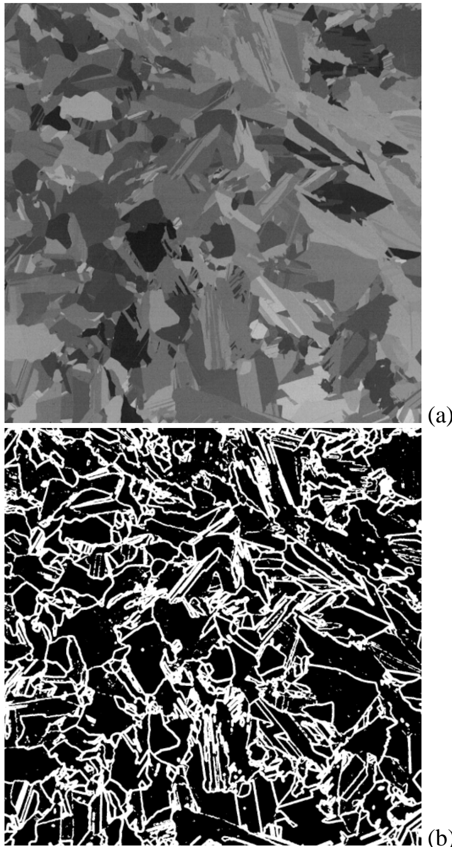

Figure 2: Scanned image of a typical mc-Si 125×125 mm² wafer before (a) and after (b) the numerical image processing.

We can then represent the results in two different ways. First, we can represent the cumulative percentage of the number of grains for each size. For example, in the red curve of Figure 3, we can read that 50% of the grains of the analyzed wafer are smaller than 0,015 cm². However, this representation does not give any information about the proportion of the wafer surface which is covered by grains smaller than 0.015 cm². A second depiction shows the cumulative percentage of the occupation of the wafers surface by grains sizes. The blue curve on the Figure 3 tells us that less than 10% of the wafer surface is occupied by grains that are smaller than 0.015 cm². This second representation seems to be more relevant to qualify the structural quality of a wafer, as the electrical properties of the solar cells will depend on the proportion of the surface occupied by small grains. We can note that this grain size distribution follows generally an exponential law.

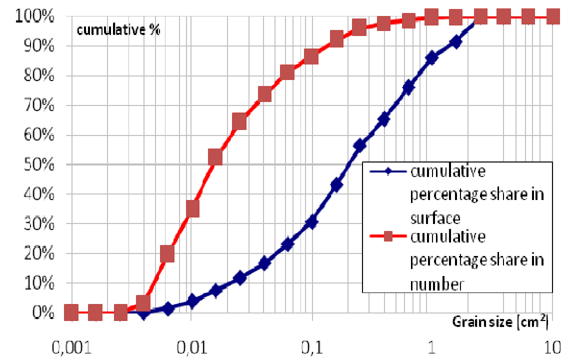

Figure 3: 2 different types of representation for the distribution of grains sizes over the wafer surface.

A calculation of the average grain size can be done for the two different types of representation. The first one represents the average of the grains sizes $\bar{s}_n$ (Eq. 1) depending on the number of grain of each size:

$$\bar{s}_n = \sum_i s_i \cdot \frac{n_i}{N} \qquad \text{Eq. 11}$$

where N is the total number of grains, n_i the number of grains with the surface S_i.

The second represents the size of the grains $\bar{s}_s$ (Eq. 2) by which the wafer's surface is in average occupied.

$$\bar{s}_s = \sum_i s_i \cdot \frac{s_i}{S} \qquad \text{Eq. 2}$$

where S is the total surface of the wafer.

In the following the grain size average will be considered as equal to $\bar{s}_s$.

3.2 Limitation of the method

Figure 4 gives an example of a scanned wafer and the related processed image for a wafer from a top part of an ingot, containing small equiaxed grains. These grains ("grit") present a very high ratio of the *grain boundary surface* to the *grain surface* , which makes them difficult to quantify with accuracy, since the grain boundaries are very close to each other and the grain surface is extremely small. Figure 5 shows the corresponding distribution curves of the two wafers presented in Figure 2 and 4. In the case of the wafer with small equiaxed grains, more

than 50% of the surface is covered with grains smaller than 0.1 cm².

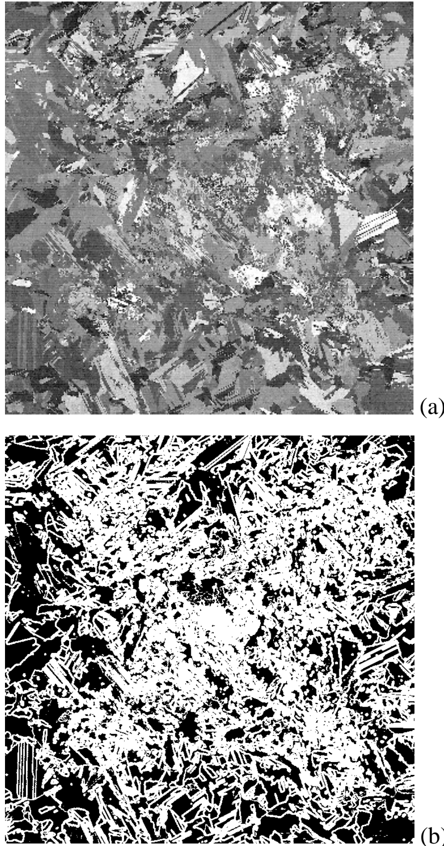

Figure 4: Scanned image of a mc-Si wafer with large areas of equiaxed small grains, before (a) and after (b) the numerical image treatment.

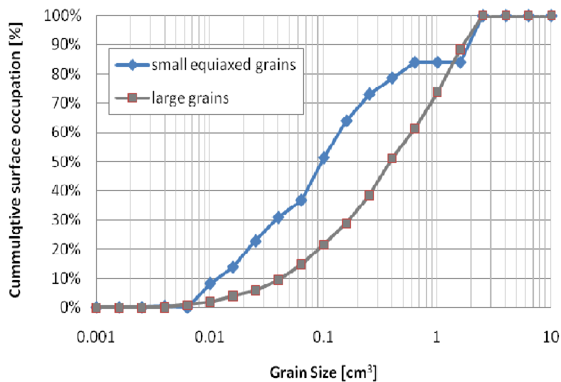

Figure 5: Cumulative surface occupation of different grain sizes for wafers with standard grain sizes and zones of small equiaxed grains.

4 RESULTS

4.1 Influence of the silicon feedstock

Grain size measurements have been carried out on wafers from different height positions of 3 different ingots, crystallized with upgraded metallurgical grade silicon (UMG-Si), solar grade silicon (SG-Si) and electronic grade silicon (EG-Si) feedstock, by applying the same crystallization conditions. The obtained results (Figure 6) show a dependence of the grains sizes on the feedstock quality, i.e. the total impurity concentration. We have measured grains size averages in a range from less than 0.1 cm² to 0.5 cm² for the UMG-Si, from 0.3 cm² to 1.6 cm² for the SoG-Si and from 0.5 cm² to 2.1 cm² for the EG-Si. This can be explained by the fact that impurities act as nucleation sites for the formation of new grains during crystallization.

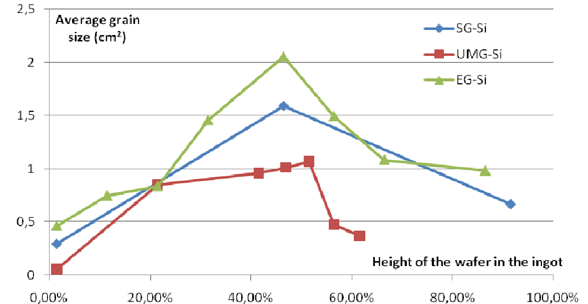

Figure 6: Evolution of the average grain size within the height of the ingot, depending on the Silicon feedstock quality.

We can also notice an evolution of the grain size depending on the vertical position of the wafers in the ingots. Grains sizes are smaller in the bottom of the ingots because of the random germination which occurs at the beginning of crystallization, due to a high cooling rate. The grains sizes then increases with the height towards the middle of the ingot and finally decreases towards the top. This can be explained by different effects: (a) segregation of impurities in the upper ingot region, (b) accumulation of non metal complexes like SiC and/or SiN in this region, (c) a slight decrease of the vertical temperature gradient at the end of the crystallization due to the presence of an insulating mass of silicon solidified..

4.2 Comparison between lifetime values and grain size

Figure 7 presents the average grain surfaces and the related average effective lifetime value, for wafer coming from an UMG-Si ingot. The effective lifetime has been measured by the QSSPCD technique, using iodine-ethanol for the wafer surface passivation.

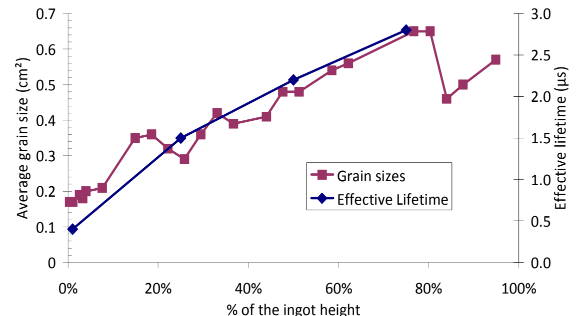

Figure 7: Comparison between average grain size and effective lifetime value (UMG-Si).

This UMG ingot contains a relatively large quantity of impurities, and exhibits smaller grains, compared to ingots from SoG Silicon. A small grain size could have a strong impact on the lifetime values, if the grain dimensions are of the same order of magnitude or smaller than the diffusion length of the minority carrier (typically

100 µm). We can thus notice that the lifetime values follow the increase of grain size throughout the top of the ingot.

4.2 Influence of the temperature profile during crystallisation

On Figure 8 is compared the average grain size for 2 UMG-Si ingot, with different temperature profiles applied during the solidification step. The ingot A presents very small grain sizes, and also exhibits some "grit" in the centre of the wafers, starting in the middle of the ingot. In such area of the wafer the average grain size remains smaller than 0.1 cm². A typical wafer from this region is presented in Figure 4. Since the grit area of the wafer is located in the centre of the wafers, the average grain size does not increase with the ingot height, and remains very low.

On ingot B the temperature profile has been improved. The average grain size is higher than for ingot A, and no more grit is visible. The average grain size thus increases with the height of the ingot.

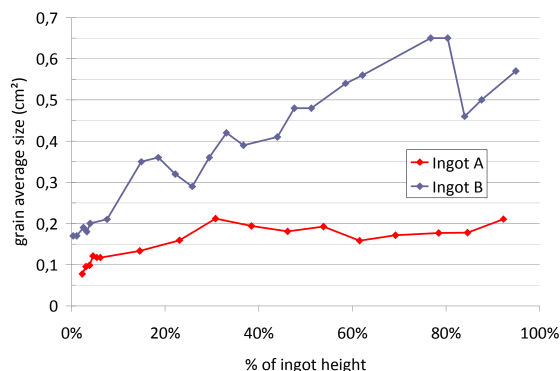

Figure 8: Influence of the temperature profile during crystallisation: comparison of wafer grain size for a standard (A) and an optimised profile (B).

4.3 Influence of other crystallization parameters

Figure 9 shows the average grain size distribution as a function of the ingot height for two ingots, both crystallized using upgraded metallurgical grade Silicon. The only difference between the two ingots A and B is a modification concerning the geometry of the Argon injection system inside the crystallisation chamber. The Argon injection towards the surface of the liquid Silicon has an influence on the carbon content inside the Silicon, since it allows evacuating both SiO and CO_2 that have formed inside the crystallisation chamber due to the presence of graphite and quartz elements inside the furnace. Ingot B was crystallised with an optimised injection geometry and flow rate and shows a larger average grain size distribution, especially in the middle section of the ingot. This tends to prove that the optimised Argon injection has been efficient enough to evacuate C from the melt and thus limit the grit formation.

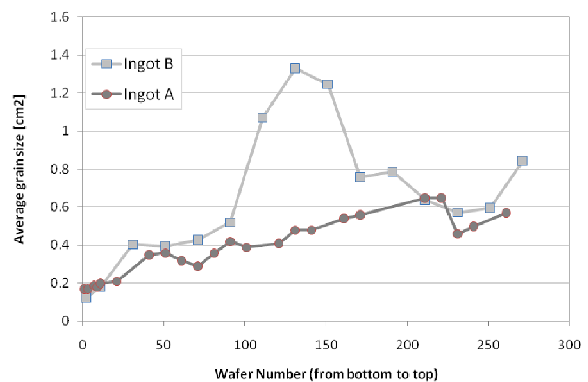

Figure 9: Average grain size distribution comparison between the "standard" process (ingot A) and a modified process (ingot B).

4 CONCLUSION

We have developed a simple method of optical analysis to quantify the crystalline quality of silicon wafer in the early stages of production. This method gives access to numerical results, which can be used in the optimisation of a directional solidification process of silicon. We have applied this method to different ingots, and used it to study the influence of the Si-feedstock quality and the thermal parameters of a new type of furnace. The results obtained have led to the improvement of the temperature and time profiles used during the crystallisation step as well as to the geometry of some furnace elements.

5 REFERENCES

[1] B. Roebuck & E.G. Bennett: *The metallographic measurement of WC grain size*. NPL Measurement Good Practice Guide No. 22 , August 1999.
[2] K.P. Mingard *et al.*: *Comparison of EBSD and conventional methods of grain size measurement of hardmetals.* Int. J. of Refractory Metals and Hard Materials, 27 (2), 2009, pp. 213-223.
[3] F. Lissalde et al.: *Innovative Crystallisation Process and Furnace for Solar Grade Silicon*, Proceedings of the 22nd European PVSEC, Milano 2007, pp. 948 – 951.
[4] J. Kraiem *et al.*: *Innovative Crystallisation of Multi-Crystalline Silicon Ingots from Different Types of Silicon Feedstock*. Proceedings of the 23rd European PVSEC, Valencia 2008, pp. 1071 – 1074.
[5] W. Rasband: *ImageJ, Image processing and Analysis in Java*. On-line: http://rsbweb.nih.gov/ij/